

Appl. No. 09/503,140
Amdt. Dated May 5, 2005
Reply to Office Action of January 5, 2005

REMARKS


Applicants have submitted this Request for Continued Examination so that the Examiner may consider the subject matter of the invention directed to the innovative error correction system described in the instant application, wherein a plurality of registers and counters are employed in conjunction with a reset signal for the purpose of determining the bit error rate. Applicants respectfully submit there is no teaching or suggestion in the prior art related to an error correction system which utilizes the now specified counters and registers which are used in conjunction with the reset signal. Furthermore, in regard to the newly submitted dependent claims, the prior art of record similarly fails to teach or suggest an error correction system wherein a selector is electrically connected between the registers and counters, or wherein a block number control change signal is employed.

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Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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 (Reg. #39,979)
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